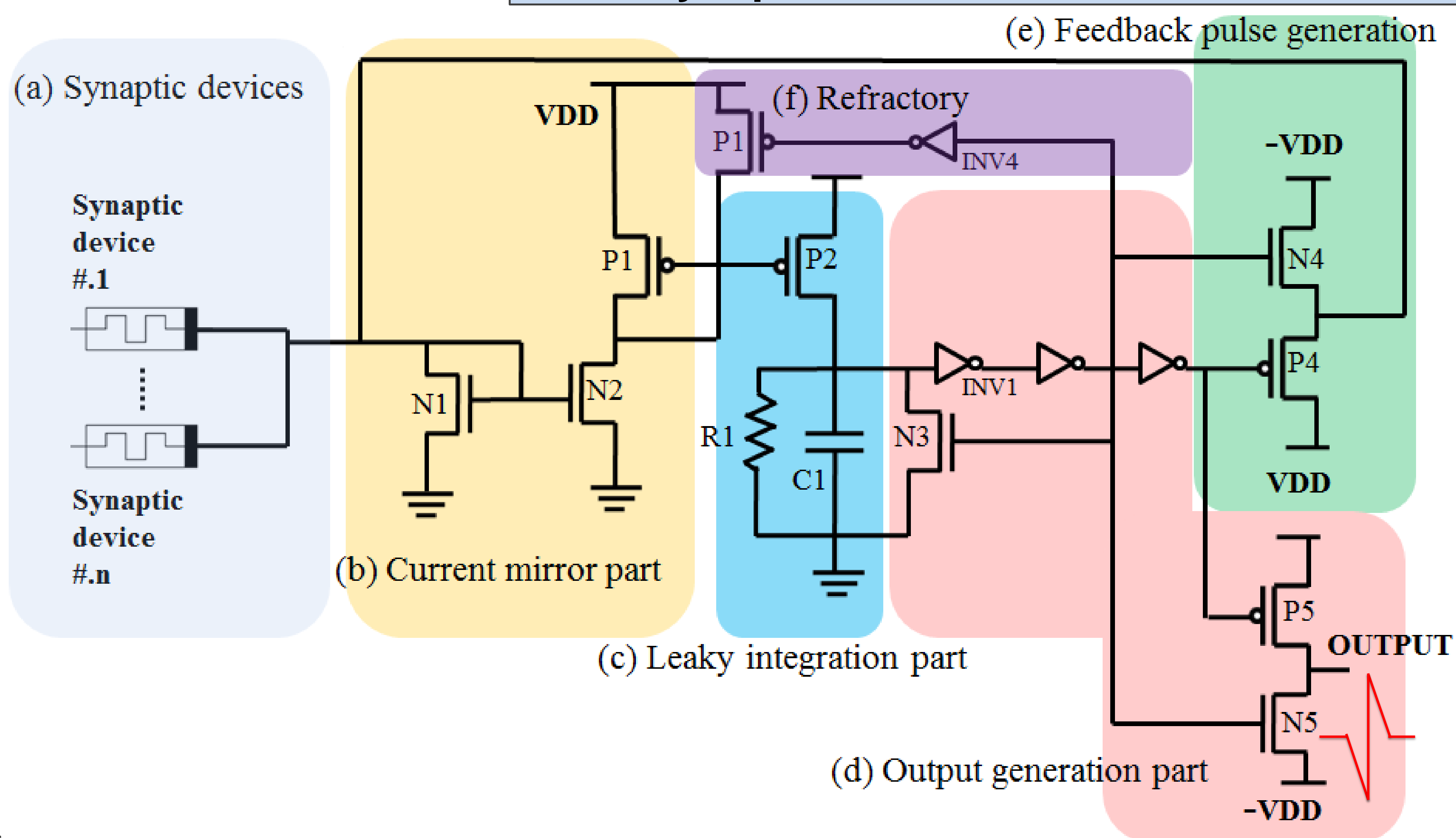


# Spiking Neural Networks with Unsupervised Learning Based on STDP Using Resistive Synaptic Devices and Analog CMOS Neuron Circuit

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## Synaptic devices and I&F neuron circuit



### Essential characteristics for SNNs

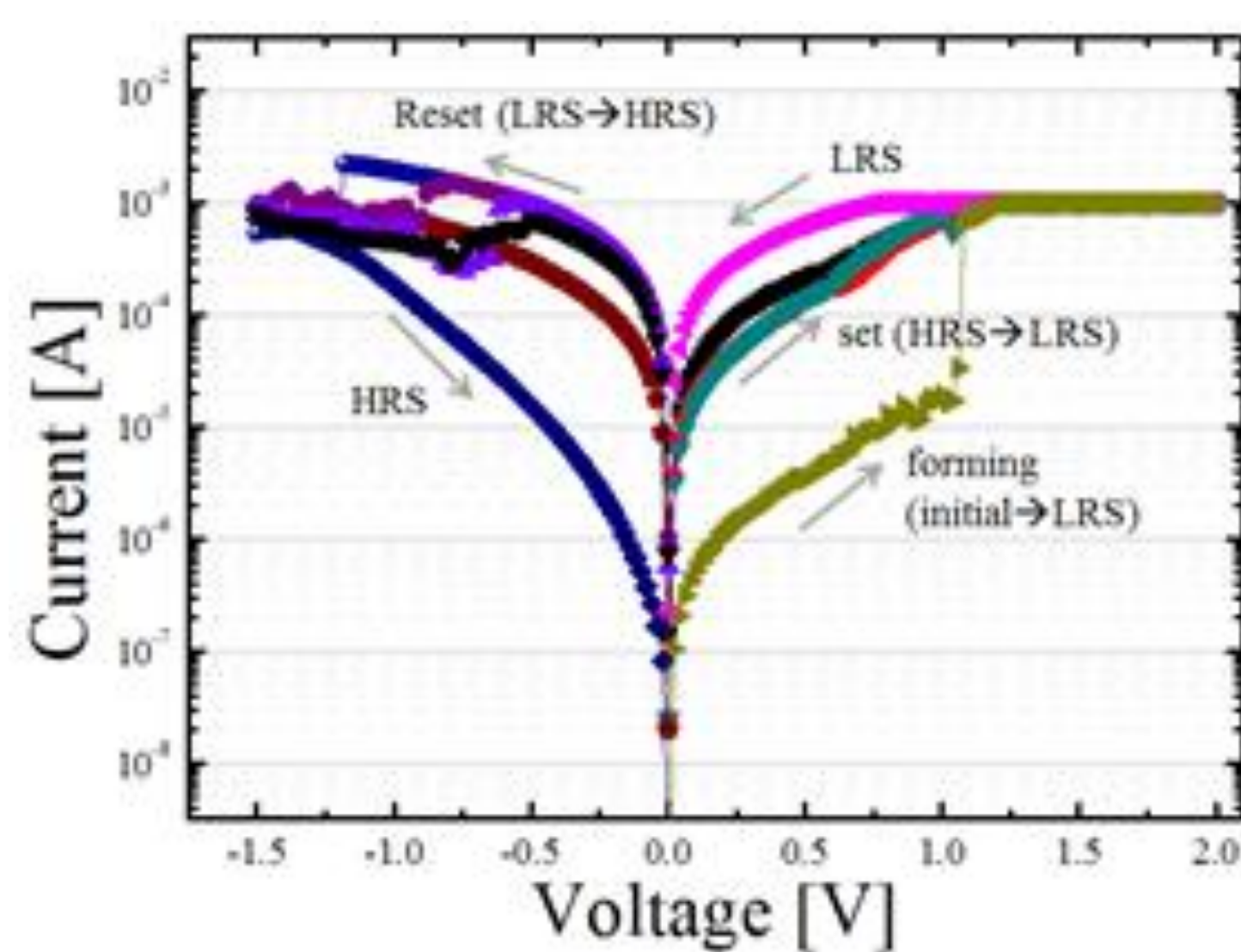
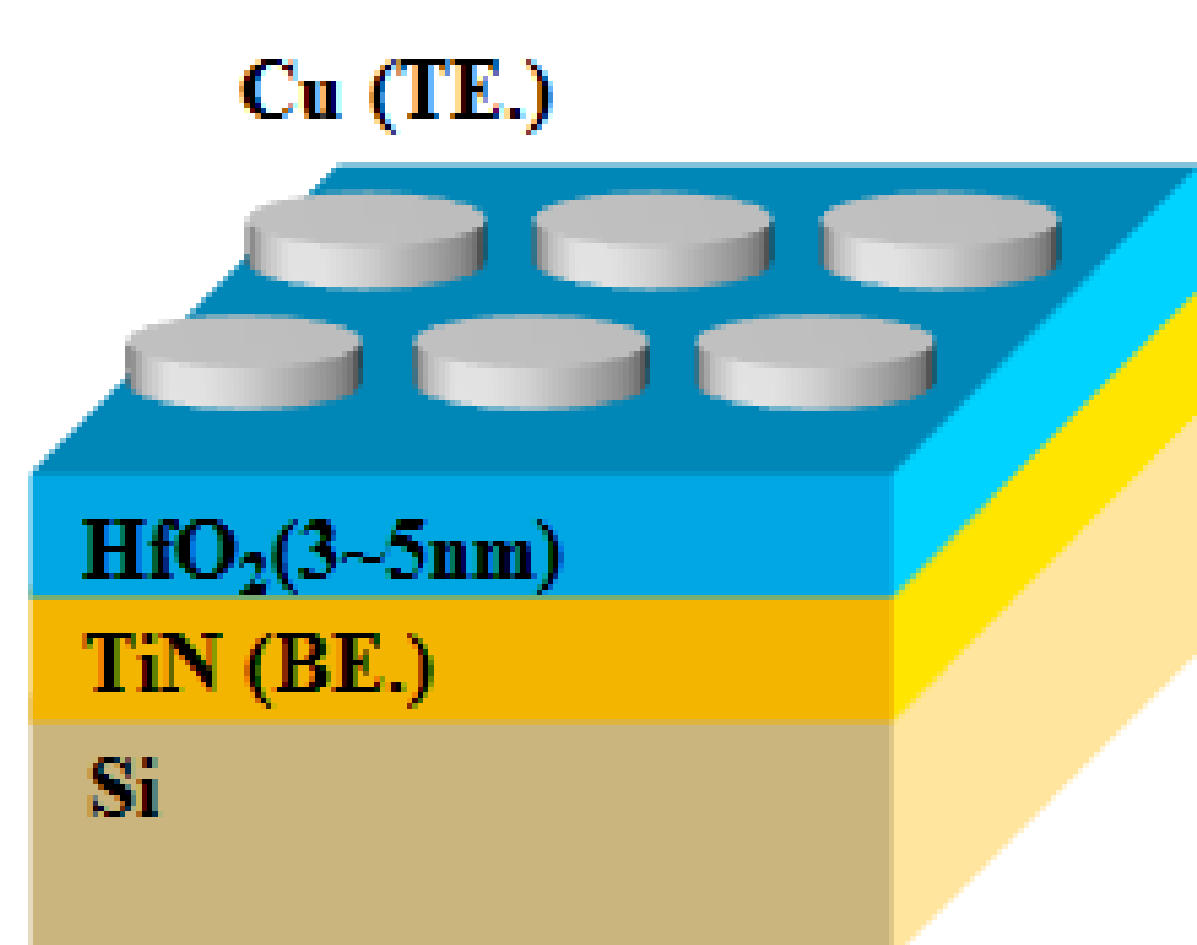
#### Synaptic device

- Gradual / multi-level switching
- HfO<sub>2</sub> resistive switching memory

#### I&F Neuron circuit

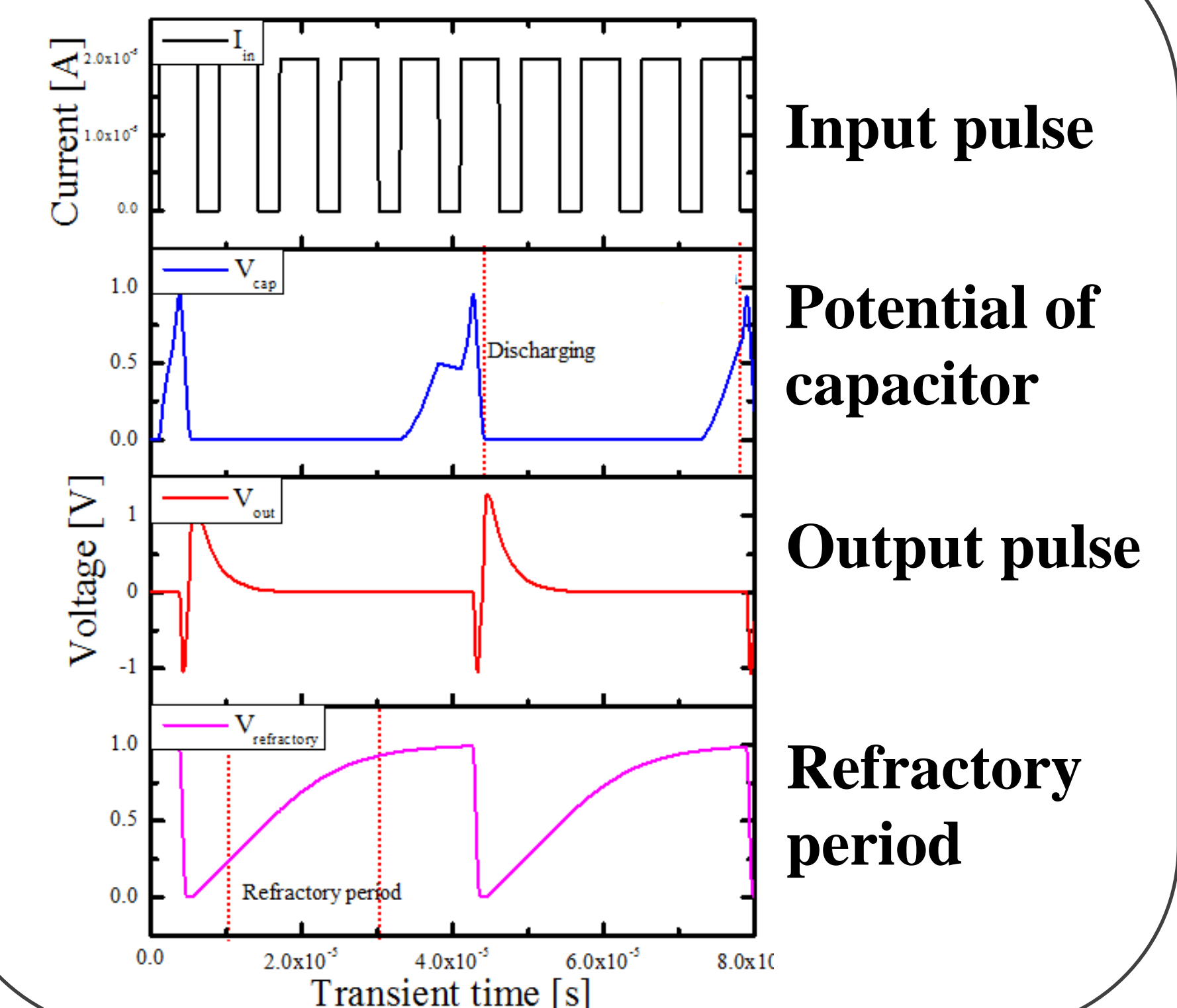
- Spatial/ Temporal leaky integration
- Asymmetric pulse generation (triangular negative and positive)
- Back-propagation for **STDP learning**
- Refractory period

## Resistive synaptic device

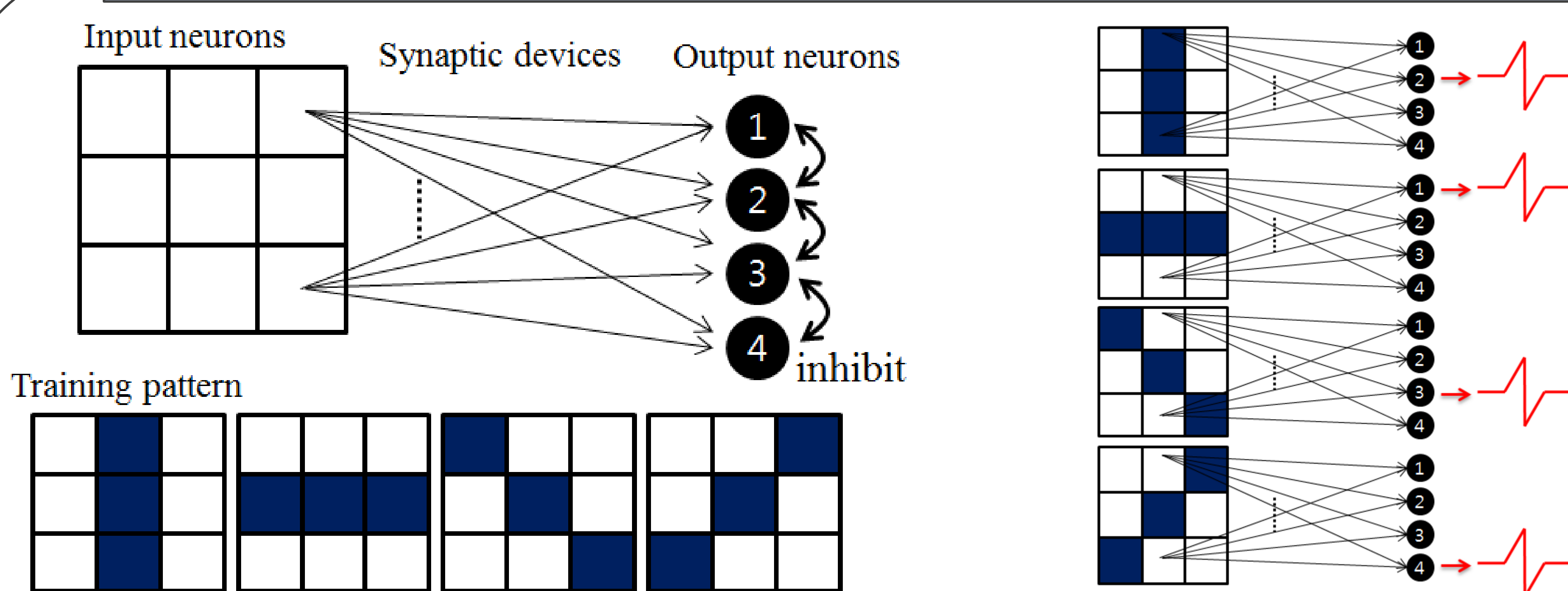


Fabricated synaptic device has HfO<sub>2</sub> switching layer were grown at T=300°C using ALD  
Measurement results of DC and transient characteristics

## Neuron circuit simulation result



## Pattern classification using SNNs



### Unsupervised, winner take all, spiking neural networks

Input patterns are applied to 1<sup>st</sup> layer → one output neuron generates action potential → the weight is modified according to the timing difference between pre and post synaptic pulses (STDP)

## Conclusion

- We developed **hardware based SNNs**. The basic computational unit in SNNs is a neuron circuit that behaves similarly to real neurons.
- We designed the neuron circuit can be operated with resistive synaptic devices.
- We verified simple pattern classification system with unsupervised, WTA, SNNs.
- Without the aid of software calculations, the hardware-based SNNs can **autonomously and efficiently control the weight updates** between neurons.

